REMARKS

The following remarks are made in response to the Non-Final Office Action mailed April 6, 2009. Claims 34-37 have been withdrawn from consideration. With this Response, claims 18, 28, 38 and 39 have been amended, and claim 42 has been added. Claims 18, 19, 22-39, 41 and 42 remain pending in the application and are presented for reconsideration and allowance.

Claim Rejections under 35 U.S.C. § 112

The Office Action rejected claims 18, 19, 22-33, 38, 39, and 41 under 35 U.S.C. § 112, second paragraph. Independent claims 18, 28, 38 and 39 have been amended along the lines suggested in the Office Action, such that the claims recite, "the passive first region having no *active* components of an integrated circuit, the test areas being arranged in the active second region, the active second region having *active* components of an integrated circuit."

The remaining claims depend on one of these claims.

In view of the above, claims 18, 19, 22-33, 38, 39, and 41 are believed to be in form for allowance. Therefore, Applicant respectfully requests that rejections to these claims under 35 U.S.C. § 112, second paragraph, be reconsidered, and that the rejections be removed and these claims be allowed.

Claim Rejections under 35 U.S.C. § 102

The Office Action rejected claims 18, 26, 27, 38, 39, and 41 under 35 U.S.C. § 102(b) as allegedly being anticipated by Kim et al. U.S. Patent No. 6,159,826 ("Kim"). Applicants respectfully traverse these rejections.'

It is well accepted that, to anticipate a claim, the cited reference must disclose each claim element, and the elements must be arranged as required in the claim. MPEP 2131 (citing *In re Bond*, 910 F.2d 831, 15 USPQ2d 1566 (Fed. Cir. 1990)).

Independent claims 18 and 39 have been amended to more clearly recite the arrangement of the through contacts included in the claim. For instance, claim 18 includes,

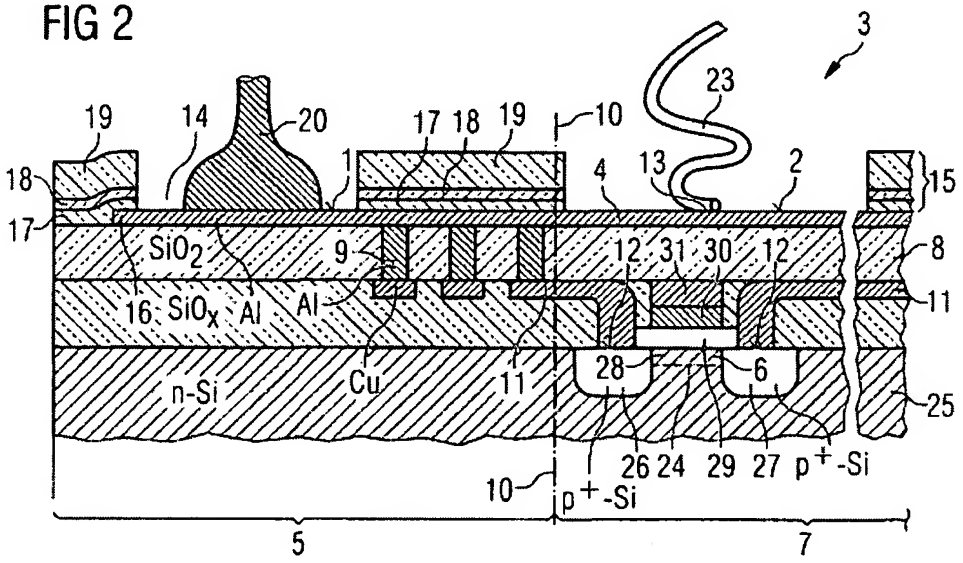
> through contacts extending through a portion of the insulating layer directly below the conduction web and extending from the conduction web to

the lower plane, the through contacts being connected to interconnects that are connected to electrodes of the components of the integrated circuit;

wherein portions of the insulating layer directly below the contact areas and the test areas are free from the through contacts.

Claim 39 has been similarly amended. An example of the recited structure is illustrated in Figure 2 of the present application, which is reproduced below.

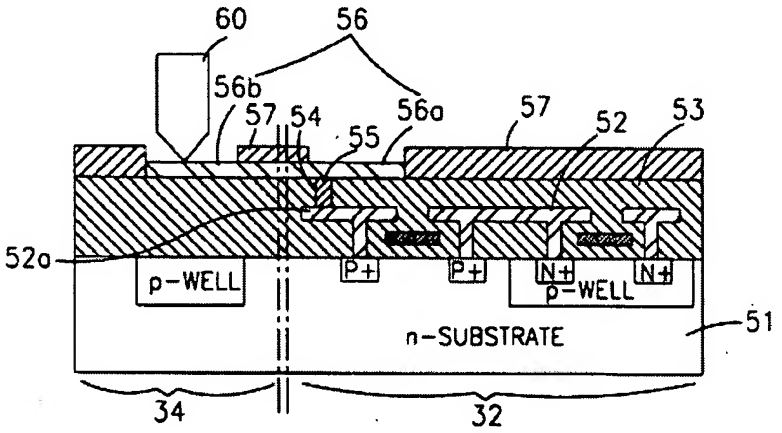
FIG 2



As shown in Figure 2, through contacts 9 are situated directly below the conduction web that joins the contact area 1 and test area 2, and the portions of the insulating layer 8 directly below the contact area 1 and test area 2 are free of through contacts.

Regarding the through contacts, the Office Action refers to Figure 5 of Kim, which is reproduced below.

FIG.5



More specifically, the Office Action equates reference 55 with the through contacts recited in the claims. The Office Action further cites references 56a and 56 of Kim regarding the test area and conduction web, respectively, recited in claim 18. As clearly shown in Figure 5 of Kim, the via hole 54/conductive region 55 of Kim is situated below the "test area" 56a, and no through contacts are situated below the "conduction web" portion of item 56 between 56a and 56b.

As such, Kim fails to disclose each element of claims 18 and 39, as well as claims 26, 27, and 41 dependent thereon.

Claim 38 is directed to a semiconductor wafer that has a plurality of semiconductor chips. Claim 38 has been amended to further include, "each of the semiconductor chips being defined by a boundary extending around the respective semiconductor chip, the contact areas and the test areas are completely situated within the boundary the respective semiconductor chip."

Figure 4 of Kim is reproduced below.

FIG.4

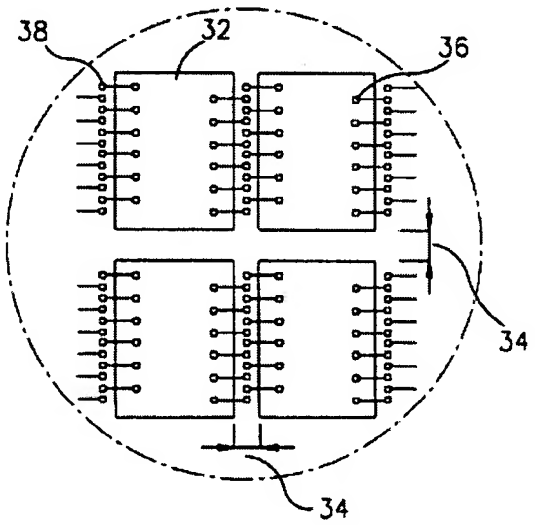


Figure 4 of Kim illustrates a portion of the wafer 30, in which "chip scribe lanes 34 are formed between the semiconductor chip portions 32." Kim at col. 3, ll. 9-10. Thus, as shown in Figure 5 of Kim reproduced above, the scribe lanes 34 are not part of the chip 32. The Office Action references the scribe lane 34 in Figure 5 of Kim with regard to the test area recited in claim 38.

Thus, the "test area" 34 of Kim is clearly not within the boundary of the semiconductor chip 32. As such, Kim does not disclose each element of claim 38.

Therefore, Applicant respectfully requests reconsideration and withdrawal of the 35 U.S.C. § 102 rejection to the claims, and requests allowance of these claims.

Claim Rejections under 35 U.S.C. § 103

The Examiner rejected claim 28 under 35 U.S.C. § 103(a) as being unpatentable over Kim. Applicants respectfully traverse this rejection.

To establish *prima facie* obviousness, all claim limitations must be considered. MPEP 2143.03 (citing *In re Wilson*, 424 F.2d 1382, 1385, (CCPA 1970). Claim 28 has been amended similarly to claim 18. As such, claim 28 includes,

> an insulating layer situated between the top side and a lower plane through contacts extending through a portion of the insulating layer directly below the conduction web and extending from the conduction web to the lower plane, the through contacts being connected to interconnects that are connected to electrodes of the components of the integrated circuit;
>
> wherein portions of the insulating layer directly below the contact areas and the test areas are free from the through contacts.

As noted above, Kim fails to disclose the recited arrangement. Since Kim fails to disclose each claim element, the Office Action fails to establish *prima facie* obviousness of claim 28.

The Office Action rejected claims 19, 22-25, and 29-33 under 35 U.S.C. § 103(a) as being unpatentable over Kim in view of Henson U.S. Patent No. 6,133,054. These claims are all dependent on either claim 18 or 28, which are believed to be allowable as set forth above. Claims 19, 22-25 and 29-33 are thus allowable for at least the same reasons.

Therefore, Applicant respectfully requests reconsideration and withdrawal of the 35 U.S.C. § 103 rejection to the claims, and requests allowance of these claims.

New Claim

Claim 42 has been added herein; no new matter has been introduced. Claim 42 depends on claim 18 and is therefore allowable for at least the same reasons. Moreover, claim 42 recites "the contact areas and the test areas are formed on the metalized area, such that the contact areas and the test areas are situated within the boundary the semiconductor chip." This is similar to elements recited in claim 38 as amended herein. As noted in the remarks concerning claim 38, the prior art passages identified in the Office Action fail to disclose these elements.

CONCLUSION

In view of the above, Applicant respectfully submits that all of the pending claims are in form for allowance. Therefore, reconsideration and withdrawal of the rejections and allowance of the claims are respectfully requested.

No fees are required under 37 C.F.R. 1.16(h)(i). However, if such fees are required, the Patent Office is hereby authorized to charge Deposit Account No. 50-0471.

The Examiner is invited to contact the Applicant's representative at the below-listed telephone numbers to facilitate prosecution of this application.

Any inquiry regarding this Amendment and Response should be directed to Mark L. Gleason at Telephone No. (612) 767-2503, Facsimile No. (612) 573-2005. In addition, all correspondence should continue to be directed to the following address:

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Respectfully submitted,

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